

## CLAIMS

What is claimed is:

- 1        1.        A method for testing a processor design, the method comprising:  
2                    searching a file that contains test results for a lot of wafers at two or more  
3        voltage levels; and  
4                    determining an optimal operational voltage based on which of the two or more  
5        voltage levels had the least test failures.
  
- 1        2.        The method of claim 1, wherein the searching the file comprises parsing the  
2        file.
  
- 1        3.        The method of claim 1, wherein the searching the file comprises opening the  
2        file and parsing the file.
  
- 1        4.        The method of claim 1, wherein the determining an optimal operational  
2        voltage comprises:  
3                    determining the number of test failures at a first voltage level;  
4                    determining the number of test failures at a second voltage level; and  
5                    determining which of the first voltage level and the second voltage level had  
6        the least test failures.
  
- 1        5.        The method of claim 1, wherein the searching the file comprises  
2        decompressing the file.

- 1        6.        A system for testing a processor design, the system comprising:  
2                a parser module for searching a file that contains test results for a lot of wafers  
3                at two or more voltage levels;  
4                a test failure calculation module for determining how many test failures  
5                occurred at the two or more voltage levels; and  
6                an optimal operational voltage module for determining which of the two or  
7                more voltage levels had the least test failures.
- 1        7.        The system of claim 6, wherein the parser module is configured to open the  
2                file.
- 1        8.        The system of claim 6, wherein the parser module, the test failure calculation  
2                module, and the optimal operational voltage module comprise software that is  
3                executed by a processor.
- 1        9.        The system of claim 6, wherein the parser module is configured to decompress  
2                the file.
- 1        10.       The system of claim 6, wherein the parser module, the test failure calculation  
2               module, and the optimal operational voltage module comprise a PERL script.

1        11.     A computer program embodied in a computer-readable medium for testing a  
2        processor design, the program comprising:

3                logic configured to search a file that contains test results for a lot of wafers at  
4        two or more voltage levels; and

5                logic configured to determine an optimal operational voltage based on which  
6        of the two or more voltage levels had the least test failures.

1        12.     The program of claim 11, wherein the logic configured to search is further  
2        configured to decompress the file.

1        13.     The program of claim 12, wherein the logic configured to search is further  
2        configured to parse the file.

1        14.     The program of claim 11, wherein the logic configured to determine an  
2        optimal operational voltage comprises logic configured to:

3                determine the number of test failures at a first voltage level;

4                determine the number of test failures at a second voltage level; and

5                determine which of the first voltage level and the second voltage level had the  
6        least test failures.

- 1        15.     A system for testing a processor design, the system comprising:
  - 2                means for searching a file that contains test results for a lot of wafers at two or
  - 3                more voltage levels; and
  - 4                means for determining an optimal operational voltage based on which of the
  - 5                two or more voltage levels had the least test failures.